**EE 310 – Lab 1 Report**

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**Problem Description**

In this lab, we have been asked to *In this lab, we are going design a state machine to display 1st, 3rd, 5th and 7th digits of your student ID on the four 7-segment displays on the Cyclone V GX Starter Kit. Upon reset, all your displays will be OFF. Then at every clock cycle, one of the displays will be ON displaying the corresponding digit. After 4 clocks, all display will be ON displaying all 4 digits, and then with the next clock the state machine will return to its initial state where all displays are OFF. This sequence will be repeated until device is turned off*

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Figure 1. Expected behavior of the circuit

**Solution Plan**

In order to solve the problem explained above, I have *decided to create a switch case and everytime the clock is hit it will move onto the next state. Then the states will call the specific bitcode for the 7 segment displays.*

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| same as before |

Figure 2. State diagram for the proposed solution

**Implementation and Test Plan**

I have implemented the solution plan explained above, by *the code is exactly what I set out to do the only difference was that I had an issue over getting the states to work. When initializing the variables I found that I initialized them incorrectly and that they did not work. After they were resolved the code worked flawlessly.*

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| //lab1 module  module lab1 ( clk , rst , ss3 , ss2 , ss1 , ss0 ) ;  input clk , rst ;  output reg [6:0] ss3 , ss2 , ss1 , ss0 ;  localparam [2:0] state\_\_\_\_ = 0 ,  state1\_\_\_ = 1 ,  state\_2\_\_ = 2 ,  state\_\_3\_ = 3 ,  state\_\_\_4 = 4 ,  state1234 = 5 ;  reg [2:0] state ;  always @ ( posedge clk ) begin // posedge clk  if ( rst ) begin // if  // Initial state  state = state\_\_\_\_ ;  end // if  else begin // else  // State transitions  case ( state )  state\_\_\_\_ : begin  state = state1\_\_\_ ;  end  state1\_\_\_ : begin  state = state\_2\_\_ ;  end  state\_2\_\_ : begin  state = state\_\_3\_ ;  end  state\_\_3\_ : begin  state = state\_\_\_4 ;  end  state\_\_\_4 : begin  state = state1234 ;  end  state1234 : begin  state = state\_\_\_\_ ;  end  default : begin  state = state\_\_\_\_ ;  end  endcase  end // else  // State actions  case ( state )  state\_\_\_\_ : begin  ss3 = 7'b1111111 ;  ss2 = 7'b1111111 ;  ss1 = 7'b1111111 ;  ss0 = 7'b1111111 ;  end  state1\_\_\_ : begin  ss3 = 7'b0100100 ;  ss2 = 7'b1111111 ;  ss1 = 7'b1111111 ;  ss0 = 7'b1111111 ;  end  state\_2\_\_ : begin  ss3 = 7'b1111111 ;  ss2 = 7'b0011000 ;  ss1 = 7'b1111111 ;  ss0 = 7'b1111111 ;  end  state\_\_3\_ : begin  ss3 = 7'b1111111 ;  ss2 = 7'b1111111 ;  ss1 = 7'b0010010 ;  ss0 = 7'b1111111 ;  end  state\_\_\_4 : begin  ss3 = 7'b1111111 ;  ss2 = 7'b1111111 ;  ss1 = 7'b1111111 ;  ss0 = 7'b1000000 ;  end  state1234 : begin  ss3 = 7'b0100100 ;  ss2 = 7'b0011000 ;  ss1 = 7'b0010010 ;  ss0 = 7'b1000000 ;  end  default : begin  ss3 = 7'b1111111 ;  ss2 = 7'b1111111 ;  ss1 = 7'b1111111 ;  ss0 = 7'b1111111 ;  end  endcase  end // posedge clk  endmodule  module lab1\_tb;  reg clk\_tb , rst\_tb ;  wire [6:0] ss3\_tb , ss2\_tb , ss1\_tb , ss0\_tb ;  localparam PER = 20 ;  lab1 dut ( clk\_tb , rst\_tb , ss3\_tb , ss2\_tb , ss1\_tb , ss0\_tb ) ;  // Generate clock  always begin  clk\_tb = 0;  #(PER/2) ;  clk\_tb = 1;  #(PER/2) ;  end  // Other stimulus  initial begin  rst\_tb = 1 ;  #PER ;  rst\_tb = 0 ;  #PER ;  #PER ;  #PER ;  #PER ;  #PER ;  #(5\*PER) ; // Simply put as many periods of delay as you need  $stop ;  end  endmodule  //--------------------------------------------------------------------------//  // Title: baseline\_pinout.v //  // Rev: Rev 1.0 //  // Last Revised: 10/13/2015 by Geraldine Baniqued //  //--------------------------------------------------------------------------//  // Description: Baseline design file contains Cyclone V GX Starter Kit //  // Board pins and I/O Standards. //  //--------------------------------------------------------------------------//  //Copyright 2012 Altera Corporation. All rights reserved. Altera products  //are protected under numerous U.S. and foreign patents, maskwork rights,  //copyrights and other intellectual property laws.  //  //This reference design file, and your use thereof, is subject to and  //governed by the terms and conditions of the applicable Altera Reference  //Design License Agreement. By using this reference design file, you  //indicate your acceptance of such terms and conditions between you and  //Altera Corporation. In the event that you do not agree with such terms and  //conditions, you may not use the reference design file. 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By making this  //reference design file available, Altera expressly does not recommend,  //suggest or require that this reference design file be used in combination  //with any other product not provided by Altera  //----------------------------------------------------------------------------  //`define ENABLE\_DDR2LP  //`define ENABLE\_HSMC\_XCVR  //`define ENABLE\_SMA  //`define ENABLE\_REFCLK  //`define ENABLE\_GPIO  module baseline\_c5gx(  ///////// ADC ///////// 1.2 V ///////  output ADC\_CONVST,  output ADC\_SCK,  output ADC\_SDI,  input ADC\_SDO,  ///////// AUD ///////// 2.5 V ///////  input AUD\_ADCDAT,  inout AUD\_ADCLRCK,  inout AUD\_BCLK,  output AUD\_DACDAT,  inout AUD\_DACLRCK,  output AUD\_XCK,  ///////// CLOCK /////////  input CLOCK\_125\_p, ///LVDS  input CLOCK\_50\_B5B, ///3.3-V LVTTL  input CLOCK\_50\_B6A,  input CLOCK\_50\_B7A, ///2.5 V  input CLOCK\_50\_B8A,  ///////// CPU /////////  input CPU\_RESET\_n, ///3.3V LVTTL  `ifdef ENABLE\_DDR2LP  ///////// DDR2LP ///////// 1.2-V HSUL ///////  output [9:0] DDR2LP\_CA,  output [1:0] DDR2LP\_CKE,  output DDR2LP\_CK\_n, ///DIFFERENTIAL 1.2-V HSUL  output DDR2LP\_CK\_p, ///DIFFERENTIAL 1.2-V HSUL  output [1:0] DDR2LP\_CS\_n,  output [3:0] DDR2LP\_DM,  inout [31:0] DDR2LP\_DQ,  inout [3:0] DDR2LP\_DQS\_n, ///DIFFERENTIAL 1.2-V HSUL  inout [3:0] DDR2LP\_DQS\_p, ///DIFFERENTIAL 1.2-V HSUL  input DDR2LP\_OCT\_RZQ, ///1.2 V  `endif /\*ENABLE\_DDR2LP\*/  `ifdef ENABLE\_GPIO  ///////// GPIO ///////// 3.3-V LVTTL ///////  inout [35:0] GPIO,  `else  ///////// HEX2 ///////// 1.2 V ///////  output [6:0] HEX2,  ///////// HEX3 ///////// 1.2 V ///////  output [6:0] HEX3,  `endif /\*ENABLE\_GPIO\*/  ///////// HDMI /////////  output HDMI\_TX\_CLK,  output [23:0] HDMI\_TX\_D,  output HDMI\_TX\_DE,  output HDMI\_TX\_HS,  input HDMI\_TX\_INT,  output HDMI\_TX\_VS,  ///////// HEX0 /////////  output [6:0] HEX0,  ///////// HEX1 /////////  output [6:0] HEX1,  ///////// HSMC ///////// 2.5 V ///////  input HSMC\_CLKIN0,  input [2:1] HSMC\_CLKIN\_n,  input [2:1] HSMC\_CLKIN\_p,  output HSMC\_CLKOUT0,  output [2:1] HSMC\_CLKOUT\_n,  output [2:1] HSMC\_CLKOUT\_p,  inout [3:0] HSMC\_D,  `ifdef ENABLE\_HSMC\_XCVR  input [3:0] HSMC\_GXB\_RX\_p, /// 1.5-V PCML  output [3:0] HSMC\_GXB\_TX\_p, /// 1.5-V PCML  `endif /\*ENABLE\_HSMC\_XCVR\*/  inout [16:0] HSMC\_RX\_n,  inout [16:0] HSMC\_RX\_p,  inout [16:0] HSMC\_TX\_n,  inout [16:0] HSMC\_TX\_p,  ///////// I2C ///////// 2.5 V ///////  output I2C\_SCL,  inout I2C\_SDA,  ///////// KEY ///////// 1.2 V ///////  input [3:0] KEY,  ///////// LEDG ///////// 2.5 V ///////  output [7:0] LEDG,  ///////// LEDR ///////// 2.5 V ///////  output [9:0] LEDR,  `ifdef ENABLE\_REFCLK  ///////// REFCLK ///////// 1.5-V PCML ///////  input REFCLK\_p0,  input REFCLK\_p1,  `endif /\*ENABLE\_REFCLK\*/  ///////// SD ///////// 3.3-V LVTTL ///////  output SD\_CLK,  inout SD\_CMD,  inout [3:0] SD\_DAT,  `ifdef ENABLE\_SMA  ///////// SMA ///////// 1.5-V PCML ///////  input SMA\_GXB\_RX\_p,  output SMA\_GXB\_TX\_p,  `endif /\*ENABLE\_SMA\*/  ///////// SRAM ///////// 3.3-V LVTTL ///////  output [17:0] SRAM\_A,  output SRAM\_CE\_n,  inout [15:0] SRAM\_D,  output SRAM\_LB\_n,  output SRAM\_OE\_n,  output SRAM\_UB\_n,  output SRAM\_WE\_n,  ///////// SW ///////// 1.2 V ///////  input [9:0] SW,  ///////// UART ///////// 2.5 V ///////  input UART\_RX,  output UART\_TX  );  lab1 dut( KEY[0] , SW[0] , HEX3 , HEX2 , HEX1 , HEX0 ) ;  endmodule |

Figure 3. Verilog code for the proposed solution

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Figure 5. Lab pictures of the running solution